HASHIGO

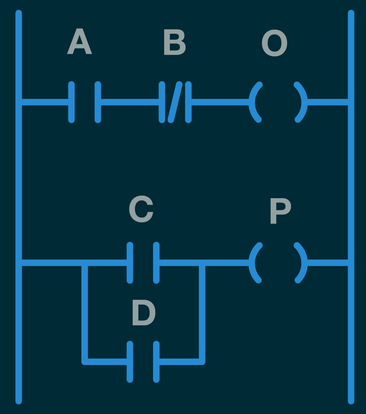
- A Ladder Logic to Verilog compiler -

Drake Brunner, Naoki Mizuno
Advisors: Dr. Peter Jamieson, Dr. Giancarlo Corti

PLC

FPGA

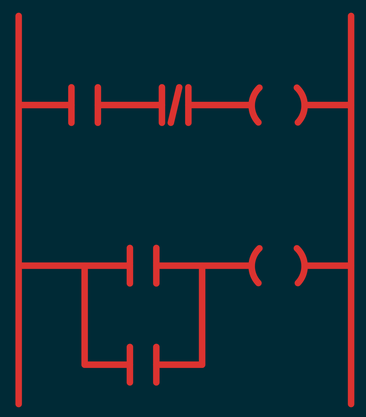
Allen-Bradley



Export

```
<Routine Name= “MainRoutine” >
    <Rung Number= “0” >
        <![XIC(A)XIO(B)OTE(O)];>
    </Rung>
    <Rung Number= “1” >
       <![XIC(C)XIC(D)]OTE(P)];>
    </Rung>
</Routine>
```

Other Dialect



Export

```
<Function Name= “MainProgram” >
    <Rung Num= “0” >
        SEQ(INC(A),INO(B))OUT(O)
    </Rung>
    <Rung Num= “1” >
        PAR(INC(C),INC(D)),OUT(P)
    </Rung>
</Function>
```

Ladder Logic

XML

The Compiler

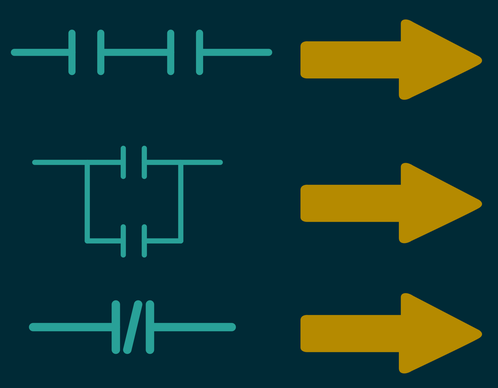
```
0: XIC(A) XIO(B) OTE(O);
1: [XIC(C), XIC(D)] OTE(P);
```

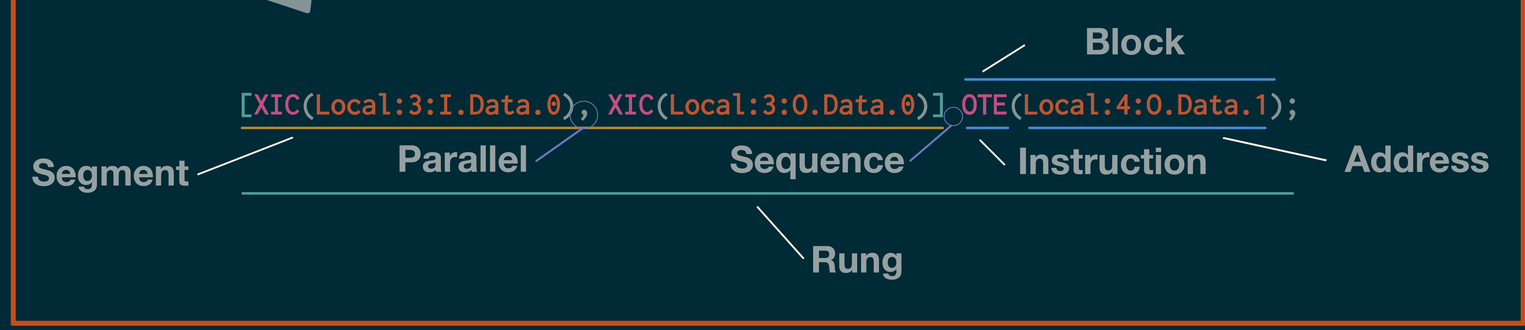
```
/* Combinational */
always @(*) begin
    o = a & ~b;
    p = c | d;
end

/* Sequential */
always @(posedge clk
        or negedge rst) begin
    case (rung)
        0: begin
            o <= a & ~b;
        end
        1: begin
            p <= c | d;
        end
    endcase
    rung <= rung + 1;
end
```

HSHG (Intermediate language)

Verilog

Ladder Logic Elements → Combinational Logic Elements





https://github.com/NigoroJr/hashigo